REMARKS

Claims 1-35 are all the claims presently pending in this application. New claims 24-35 are added.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

The Examiner previously objected to claim 3. Since the Examiner does not maintain this objection in the latest Office Action, Applicant considers that it has been withdrawn.

Claim 22 stands rejected under 35 U.S.C. §102(e) as being anticipated by Levy (U.S. Patent No. 5,923,892). Claims 1, 2, 4-16, and 18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Levy, further in view of Schmidt et al. (U.S. Patent No. 5,727,227). Claim 3 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Levy;/Schmidt, further in view of Irwin (U.S. Patent No. 4,695,945). Claim 17 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Levy/Schmidt, further in view of Yamanaka (U.S. Patent No. 4,774,625). Claims 19 and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Levy, further in view of Irwin (U.S. Patent No. 4,695,945). Claim 21 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Levy, further in view of Irwin and Schmidt.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

As described in, for example new claim 24, the claimed invention is directed to a microprocessor system for executing instructions described in a program. A main processor executes by means of hardware those instructions which belong to a first instruction set and executes by means of software those instructions which belong to a second instruction set.

A co-processor is operative under the control of the main processor for autonomously fetching an instruction belonging to the second instruction set to execute the fetched instruction by means of hardware of the co-processor. The coprocessor is provided with a

stack memory for holding data generated in the course of execution of an instruction which belongs to the second instruction set, a stack pointer for holding an address of the most recent data in the stack memory, a program counter for holding an address of an instruction which is currently processed and belongs to the second instruction set, and an updating circuit for, in response to the detection of an encounter with a specific instruction among instructions belonging to the second instruction set for which data presently under the control of the main processor needs to be handled, issuing a notification of the encounter to the main processor to request the main processor to execute the specific instruction, and for updating the stack pointer in the stack memory and the program counter.

In contrast, in conventional computer architecture, the main processor takes over the complete execution of the commands.

II. THE PRIOR ART REJECTIONS

A co-processor according to the present invention is provided with an updating circuit which, in response to the detection of an encounter with a specific instruction among instructions belonging to a second instruction set for which data presently under the control of a main processor needs to be handled, issues a notification of the encounter to the main processor to thereby request the main processor to execute the specific instruction, and updates a stack pointer in a stack memory and a program counter.

Employing such a structure makes it possible to execute a specific set of instructions, that is, the second instruction set, at a high speed while limiting an increase of the circuitry size. In addition, software executed by the main processor can be used effectively, and the size of the hardware of the co-processor is maintained as small as possible.

In contrast, *Levy* fails to disclose or suggest the structure of the present invention described above. *Levy* discloses that a host processor 22 executes an instruction in response to a request from a coprocessor 38 (column 6, line 6, through column 7, line 5). However, *Levy* merely discloses Java instructions such as array allocation operations as a condition for the coprocessor requesting the host processor to execute an instruction (column 6, last paragraph).

The co-processor according to the present invention determines whether the co-processor can execute a fetched instruction in an unassisted manner. When the co-processor

encounters an instruction that cannot be executed by the co-processor itself, this instruction is executed by software running on the main processor, and the updating process of the values of the program counter and the stack pointer accompanying with the execution of this instruction is executed by the hardware of the co-processor. As a result, it is not necessary for the main processor to update the values of the program counter and the stack pointer while the software running on the main processor is executing an instruction requested from the co-processor. Therefore, a beneficial effect is obtained that the processing load on the software running on the main processor can be decreased.

Applicant submits that the prior art of record makes no suggestion for this combination of computer architecture.

Relative to the claims previously presented, the Examiner alleges that Levy anticipates the invention of claim 22, and when combined with Schmidt, renders obvious claims 1, 2, 4-16, and 18. The Examiner also alleges that Levy/Schmidt, when combined with Irwin, renders obvious claim 3 and, when combined with Yamanaka, renders obvious claim 17. The Examiner further alleges that Levy, when combined with Irwin, renders obvious claims 19 and 20, and, when further combined with Schmidt, renders obvious claim 21.

Applicant submits, however, that, since the Examiner's interpretation of these prior art references is constraint to an interpretation consistent to that of a person of ordinary skill in the art, there are elements of the invention of these claims which are neither taught nor suggested by Levy, either alone or in combination with any or all of the prior art currently of record. Applicant again submits that the combinations of references are improper, thereby establishing that the Examiner has not met the initial burden of a *prima facie* rejection.

As Applicant previously explained, although the Examiner can reasonably consider that the embodiment discussed at lines 48-51 of column 9 and lines 8-36 of column 10 of Levy, by reason of omitting some of the instructions to simplify the coprocessor, is similar in some respects to the present invention, the mechanism in Levy differs. Applicant further submits that the modification of Levy by Schmidt would not remedy the deficiency of Levy and, indeed, would change entirely the principle of operation of Levy.

More specifically, the Examiner concedes that Levy does not use the technique of interrupt vectors. Instead, as clearly described at lines 22-28 of column 10, the main processor in Levy simply retrieves the current operational state of the co-processor via the

expansion bus and, using this retrieved state information, executes the exception instruction once it has determined that the co-processor has made a request, by checking the instruction trap flag. As clearly explained at lines 55-60 of column 7 and at lines 51-59 of column 9, the instruction trap flag is used in Levy to signal to the host processor when it is expected to provide the computations not possible by the co-processor.

As explained beginning at line 5 of page 26, by using the interrupt vector concept, the present invention exemplarily can eliminate up to ten of the forty operation clocks conventionally required for software implementation of an instruction.

That is, these ten steps are needed in the conventional method used in Levy, in which the host processor must decipher the required operation to be executed by the data in the current operational state of the co-processor, as transmitted to the host computer when it has been requested to execute an instruction.

Therefore, in the present invention, for those most frequently-used instructions that are represented by unique vector interrupts, the execution by the main processor is faster than would be done in Levy. Moreover, as further clarified in claim 22, the present invention vector interrupt scheme includes the capability to generate a vector interrupt for any one of multiple instructions, with the main processor using additional information, such as the contents of the program counter, to determine which of the possible instructions is specifically to be executed.

Because Levy does not use the technique of (dedicated) signal line(s) for a vector interrupt, Applicant submits that it fails to anticipate the present invention defined by claim 22. Applicant submits that one of ordinary skill would readily understand the difference between a flag bit in a digital data word and a signal line used for communicating a vector interrupt. However, to expedite prosecution, Applicant has further amended claim 22 to highlight the significance of the vector interrupt scheme used in the present invention, for the benefit of the Examiner.

Hence, turning to the clear language of the claim, in Levy there is no teaching or suggestion of: "... a main processor including an interrupt request reception circuit to decode an interrupt vector, said interrupt vector comprising a dedicated interrupt vector component and a common interrupt request component; a co-processor operative under the control of said main processor for autonomously fetching and executing an instruction, said co-processor

including an interrupt request generation circuit for encoding said interrupt vector; ... wherein said dedicated interrupt vector component comprises an encoding for a specific interrupt handler to be executed by said main processor and said common interrupt request component provides a request for one of a plurality of interrupt handlers to be specifically identified by additional information", as required by claim 22.

Relative to the rejection for claim 1, as explained below, although the Examiner urges a combination of Schmidt with Levy in order to incorporate interrupt vectors into Levy, such combination would not overcome the deficiency of using dedicated signal line(s). Nor would modification of Levy by Schmidt be possible without changing the principle of operation of Levy.

First, Applicant submits that the rejection currently of record fails to explain precisely how the Examiner intends that Levy be modified and why one of ordinary skill in the art would be motivated to make any modifications. In Paragraph 8 on page 4 of the Office Acition, the rejection currently of record merely conclusory statements, as follows:

> *"Levy has not taught an interrupt vector. Schmidt has taught interrupt vectors (Schmidt column 3, lines 4-42). A person of ordinary skill in the art at the time the invention was made would have recognized that an interrupt vector identifies information, including the address of the interrupt service routine, needed in order to execute the interrupt service routine. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the interrupt vector of Schmidt in the device of Levy to provide the information needed to access the interrupt service routine."* (Emphasis by Applicant)

Applicant respectfully submits that the above conclusory statement fails to meet the initial burden of a *prima facie* rejection.

That is, the Examiner forgets that Levy already has a method to determine which software operation is to be performed by the host processor. Therefore, in order to meet the initial burden, the Examiner would have to provide a reasonable motivation to modify and/or replace the system already being used in Levy. As pointed out above, compared to Levy, the vector interrupt scheme of the present invention permits exemplarily a savings of ten out of forty clock cycles for those instructions pre-identified as being those instructions that will be most frequently requested to be executed by software by the main processor.

Second, "... would have recognized ..." is not the proper legal standard for an obviousness rejection. The proper legal standard is whether the prior art provide at least a suggestion to make the modification. In the specific evaluation, the Examiner, therefore, would have to explain why one would be motivated to replace the method described at lines 22-36 of column 10 of Levy to become a method based on a vector interrupt method. The rejection currently of record fails to provide any reasonable motivation to modify Levy except the conclusory statement that one of ordinary skill would have "recognized that an interrupt vector identifies information...."

Moreover, Applicant submits that the following guidelines in MPEP §2143.01 precludes such conclusory analysis:

> - "*The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.*"
> - "*A statement that modification of the prior art to meet the claimed invention would have been " 'well within the ordinary skill of the art at the time the claimed invention was made' " because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references.*

Third, the Examiner has fallen into the classic logic trap of a circular reasoning. That is, in the rejection currently of record, the motivation to modify Levy is that one would thereby obtain the benefit of having made the modification. Under this circular logic, everything would be obvious.

Applicant submits that the correct legal standard is that the motivation to modify come from the prior art itself and that this legal standard requires more than merely describing the effect of having made the modification.

Moreover, as Applicant previously submitted, modification of the method described at lines 22-36 of column 10 would change the principle of operation of Levy, as well as the basic architecture shown in Figure 3.

That is, in spite of the Examiner's allegation in Paragraph 7b that the description at line 50 of column 6 through line 24 of column 7 describes an interrupt request reception circuit, Applicant respectfully traverses this characterization. Applicant submits that the cited description merely describes that the host processor has the capability of processing specific

instructions. There is no suggestion whatsoever of a specialized "interrupt request reception circuit". Indeed, Applicant submits that, to one of ordinary skill in the art, the description at lines 22-36 of column 10 clearly indicates that the exception processing is strictly software (e.g., as based on the "instruction trap flag", presumed to be a bit in a digital data word) and that no interrupt request reception circuit is involved.

Therefore, the software technique described at lines 22-36 of column 10 would have to be replaced or modified by one that includes an interrupt request reception circuit not currently present in the architecture shown in Figure 3.

Second, in spite of the Examiner's allegation in Paragraph 7d that Levy at lines 21-24 of column 8, lines 46-59 of column 9, and lines 4-36 of column 10 indicates an interrupt request generation circuit that uses (dedicated) signal lines, Applicant respectfully submits that one of ordinary skill in the art would not agree with the Examiner. The description at lines 24-33 of column 8, lines 54-59 of column 9, and lines 22-36 of column 10 clearly describe that the exception in which the co-processor requests assistance of the host processor is achieved by the instruction trap flag bit, not by dedicated signal lines.

Therefore, the co-processor interface module 54 shown in Figure 3 would have to be modified to incorporate a circuit to interface with dedicated signal lines having vector interrupt information.

All of the above changes would cause the principle of operation of Levy to be changed, and such change of principle is improper under MPEP §2143.01.

Perhaps even more important, the Examiner fails to explain exactly how Levy is to be modified in accordance with Schmidt. As best understood, the Examiner considers that the "interrupt vector concept" is to be imported from Schmidt into Levy as an abstract idea.

Applicant respectfully submits that, just as abstract ideas are precluded by 35 USC §101 as being non-statutory subject matter, the Examiner is likewise precluded from considering elements from an entirely different invention as being abstract ideas to be summarily imported into another invention, simply to provide the benefit described by the abstract idea.

Moreover, even if Schmidt were to be used as a model to incorporate "interrupt vectors" into Levy, the implementation of interrupt vectors described in Schmidt would defeat the purpose of Levy.

That is, according to the Abstract and the description at lines 23-43 of column 5, Schmidt teaches using an interrupt coprocessor 30 is introduced for the purpose of performing the interrupt, rather than having the microprocessor 12 take time to perform the interrupt. Alternatively, if the interrupt coprocessor 30 is incapable of performing the interrupt, it signals the microprocessor 12 to do the execution.

Therefore, based on the model provided by Schmidt, the Examiner needs to update the rejection currently of record to describe how an interrupt coprocessor 30 is to be incorporated into Levy. Applicant submits that, first, one of ordinary skill in the art would not be motivated to introduce a third coprocessor (e.g., an interrupt coprocessor 30) into the system of Levy for purpose of performing a task already being done.

Second, should the Examiner decide that a third coprocessor would be useful for relieving the host processor from performing the interrupt, then it is noted that the purpose of the host processor 22 of Levy would thereby be defeated, since the purpose of this host processor was to be able to perform the instructions beyond the capability of the co-processor 38.

Under either scenario, the incorporation of the interrupt coprocessor 30 of Schmidt would change the principle of operation of Levy. Again, such change of principle of operation is precluded by MPEP: "The proposed modification cannot change the principle of operation of a reference".

The Irwin and Yamanaka references are introduced for reasons unrelated to this deficiency in Levy and, therefore, do not overcome this deficiency in Levy.

Hence, turning to the clear language of claim 1, there is no teaching or suggestion in Levy of: "... said main processor including an interrupt request reception circuit to decode an interrupt vector for said execution of an instruction of said second instruction set by using an interrupt handler; ... said co-processor including an interrupt request generation circuit for encoding said interrupt vector, said interrupt request generation circuit being connected to said interrupt request reception circuit by at least one signal line and allowing an interrupt vector address to be identified in said main processor."

In response to the Examiner's comments in Paragraphs 28 and 29 and her reliance upon *In re Oetiker*, Applicant respectfully request that the Examiner expand her summary of the case to include the facts of that case and the holding (e.g., that the Federal Circuit reversed

the Board's decision and held that the prior art references were improperly combined and that the initial burden was thereby not met). In the *Oetiker* holding, Judge Newman wrote:

> *In order to rely on a reference as a basis for rejection of the applicant's invention, the reference must either be in the field of the applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned. [citations omitted] Patent examination is necessarily conducted by hindsight, with complete knowledge of the applicant's invention, and the courts have recognized the subjective aspects of determining whether an inventor would reasonably be motivated to go to the field in which the examiner found the reference, in order to solve the problem confronting the inventor. We have reminded ourselves and the PTO that it is necessary to consider "the reality of the circumstances" [citations omitted] - in other words, common sense - in deciding in which fields a person of ordinary skill would reasonably be expected to look for a solution to the problem facing the inventor.*
>
> *It has not been shown that a person of ordinary skill, seeking to solve a problem of fastening a hose clamp, would reasonably be expected or motivated to look to fasteners for garments. The combination of elements from non-analogous sources, in a manner that reconstructs the applicant's invention only with the benefit of hindsight, is insufficient to present a* prima facie *case of obviousness. There must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination. That knowledge can not come from the applicant's invention itself."*

Judge Rader states this requirement in a more stringent manner in the recent Federal Circuit Court of Appeals holding in *Ruiz v. A.B. Chance Co.*, Federal Cir., No. 03-1333, January 29, 2004:

> *"In making the assessment of differences, section 103 specifically requires consideration of the claimed invention "as a whole." Inventions typically are new combinations of existing principles or features. Envtl. Designs, Ltd. v. Union Oil Co., 713 F.2d 693, 698 (Fed. Cir. 1983) (noting that "virtually all [inventions] are combinations of old elements."). The "as a whole" instruction in title 35 prevents evaluation of the invention part by part. Without this important requirement, an obviousness assessment might break an invention into its component parts (A + B + C), then find a prior art reference containing A, another containing B, and another containing C, and on that basis alone declare the invention obvious. This form of hindsight reasoning, using the invention as a roadmap to find its prior art components, would discount the value of combining various existing features or principles in a new way to achieve a new result - often the very definition of invention."*

Although the holding in the *Ruiz* case left undisturbed, under the "clear error" standard of review, the conclusion of the District Court that the prior art references were properly

combinable, it specifically explained that it declined to reverse this conclusion because "... *the two references address precisely the same problem* ... " (emphasis by Applicants)

This aspect of the *Ruiz* holding, in which precisely the same problem is being addressed by both references, is not present in the Levy and Schmidt references used in the prior art evaluation of the present Application. That is, in Levy, the problem addressed is similar to that of the present invention in that it provides two processors, a host processor and a co-processor, with the host processor providing software implementations of specific instruction not available on the co-processor.

To arrive at the present invention described by the independent claims, the Examiner concedes that Levy would have to be "improved" to replace the software-implemented exception processing by a method involving vector interrupts.

In contrast, as described at lines 33-42 of column 3 of Schmidt, the problem being addressed in that reference is that of reducing the large number of clock cycles to execute interrupt structures, specifically vector interrupt structures. Therefore, the present motivation to combine Schmidt with Levy presupposes the desireability of replacing the scheme in Levy by an interrupt vector scheme.

Applicant submits that, absent some suggestion in Levy to substitute the software-implemented method with one involving vector interrupts and absent some suggestion in Schmidt that vector interrupts would improve the software-implemented interrupt method of Levy, one of ordinary skill in the art would have no motivation to modify Levy and no motivation to search, absent hindsight, the art area that includes Schmidt, let alone a motivation to modify Levy in the manner of incorporating a second co-processor dedicated to vector interrupt processing.

Without either such suggestion, Applicant submits that the evaluation currently of record lacks the "common sense" that Judge Newman describes as being necessary for a *prima facie* rejection.

Applicant submits that Judge Newman's "common sense standard" precludes the practice common among Examiners to consider prior art elements as abstract ideas to be incorporated as missing elements in a claimed invention because their incorporation would provide the benefit achievable by the abstract idea.

Moreover, given the different purposes of Schmidt and Levy, Applicant further submits that, in accordance with Judge Rader's requirement of "addressing precisely the same problem", one of ordinary skill in the art would have no reason whatsoever to search for Schmidt, let alone incorporate an addition processor dedicated to executing vector interrupts (thereby, additionally defeating the purpose of the host processor of Levy).

Therefore, prior to proceeding to appeal, Applicant respectfully requests that the Examiner clarify the rejection currently of record to provide a proper motivation to modify Levy to incorporate vector interrupts, given that Levy already has a method that performs the exception processing in a manner different from vector interrupts. Applicant again submits that, absent such clarification on the record, the rejection currently of record fails to meet the Examiner's initial burden, as clearly defined by Judge Newman in *In re Oetiker*, upon which holding the Examiner relies so heavily.

Additionally, Applicant traverses the following points in the rejection.

Relative to the urged combination of Yamanaka with Levy, such combination would be improper since the Yamanaka operation processors 17a, 17b, 17c are slave processing units, rather than the autonomous co-processors of Levy. Again, as mentioned above, the Examiner cannot simply consider elements as abstract ideas to be incorporated without any "common sense" (e.g., the engineering reality of the prior art references).

Relative to claim 4, Applicant again submits that Schmidt does not teach the technique in which dedicated interrupt vectors are used for the more-frequently-executed instructions.

Relative to claim 5, Applicant again submits that Schmidt does not teach the technique in which multiple instructions are assigned to one interrupt vector. The description at lines 4-42 of colum 3 of Schmidt describes the conventional concept of a single interrupt for each interrupt vector. In contrast, the present invention includes an embodiment in which a single interrupt vector refers to alternative interrupts.

Relative to claims 6, Applicant again submits that Schmidt does not teach a priority among multiple interrupt vectors, let alone using dedicated interrupt vectors for higher priority interrupts and multiple-instruction interrupt vectors for lessor priority interrupts.

Relative to claim 10, Applicant again submits that Levy does not have a status register in the coprocessor 38 that the host processor 22 periodically accesses to check whether the coprocessor has encountered an exception instruction. The closest analogy in Levy is the

instruction trap flag described at lines 54-59 of column 9. However, the content of this flag is directly presented to the main processor. Therefore, the register in Levy would be located in the host processor 22, not the coprocessor 38. Moreover, in Levy, the host processor 22 does not "periodically access" a register in the coprocessor 38 to determine whether the coprocessor is asking for assistance, as the plain language of the claim requires.

Relative to claim 14, Applicant again submits that Levy does not have a stack-top register (e.g., see Figures 8A, 8B, and 10 and item 270A of Figure 11 of the present application) that is utilized by exemplary embodiments of the present invention.

Relative to claim 15, Applicant again submits that Levy, therefore, also cannot have a cache memory provided between the stack memory and the stack-top register (e.g., see item 270C in Figure 11 of the present application), as used in specific exemplary embodiments of the present invention. Similarly, Levy inherently fails to describe the definition in claim 16.

Applicant again notes that the Examiner is required to address the plain language of the description of the claimed invention, using an interpretation consistent with one that one of ordinary skill in the art would agree. The latest Office Action, dated June 15, 2004, makes no attempt to update the original rejection to address the above-identified specific deficiencies previously brought to the Examiner's attention. Applicant respectfully requests that the Examiner properly address these specific deficiencies on the record prior to proceeding to appeal, in accordance with MPEP §707.07(f).

III. FORMAL MATTERS AND CONCLUSION

Applicant gratefully acknowledges the Examiner's presumed withdrawal of the previous drawing objection.

In view of the foregoing, Applicant submits that claims 1-35, all the claims presently pending in the application, are patentably distinct over the prior art of record and that the application is in condition for allowance. The Examiner is respectfully requested to pass the application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 12/7/04

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